

## Moore's Law Revisited

***“Moore’s Law’s dead...It’s completely over.”***  
***Jensen Huang, Nvidia CEO (Sept. 21, 2022)***

As Moore's law and the nascent integrated circuits were instrumental to enhance the data processing capabilities from the 1970's onwards, in particular in the growing scientific satellite production in the USA and abroad the Editor was wondering whether the law still holds up or if there are any indications - although the computing capabilities are accelerating enormously, that Moore's postulations become harder to be maintained and is reaching its limits.

In order to find out chatGPT was consulted and prompted with the following question:

**Are there any indications as to whether Moore's Law still holds for 2025 and the next ten years?**

**ChatGPT said:**

There's a lot of debate among experts about whether Moore's Law will meaningfully continue through 2025–2035. In short: there are indications it is weakening (in its original form), but many believe the spirit of it (i.e. continued exponential progress in computing power, cost, efficiency) will persist—albeit via different technologies, architectures, and trade-offs. Below are the main arguments, evidence, and outlooks.

**What is Moore's Law, and how is it “holding up” now**

- **Moore's Law** originally observed that the number of transistors on an integrated circuit doubles about every two years (later recast somewhat loosely as “every ~18–24 months”) while cost per transistor falls. [Wikipedia+2Splunk+2](#)
- Over recent years, key physical, economic, and design constraints have made it harder to maintain that doubling at the same rate. Things like leakage current, quantum tunneling, heat dissipation, yield issues, cost of new fabs and lithography tools, etc. [InSemi Tech+3PatentPC+3Live Science+3](#)

**Signs that Moore's Law is slowing / reaching limits**

Several recent indicators suggest that the original pace is hard to sustain.

1. **Transistor cost per unit and scaling complications**
  - While transistor count (density) is still increasing, the reduction in cost per transistor (especially at advanced process nodes) has slowed down or reversed in some cases. The improvements are no longer as “cheap” as before. [Live Science+3asteriskmag.com+3PatentPC+3](#)
  - At nodes beyond ~5nm or 3nm, fabrication complexity, yield, and tool costs grow steeply. Physical issues (e.g. electrostatics, leakage) are harder to manage. [PatentPC+2InSemi Tech+2](#)
2. **Diminishing returns / slower doubling**
  - Some semiconductor companies and experts suggest that instead of a doubling every two years, we may now be seeing slower rates. [Wikipedia+2Live Science+2](#)
  - Also, performance gains from more transistors aren't scaling linearly because other bottlenecks (wiring/interconnect, memory bandwidth, heat, energy efficiency) intervene.
3. **Physical/material limits**
  - When transistor gate lengths approach a few atoms, quantum effects, variability, thermal issues become large challenges. There are physical limits (both in materials and in what is manufacturable at scale) that cannot be ignored. [PatentPC+2InSemi Tech+2](#)

- Alternative materials (2D materials, non-silicon channels, Gate-All-Around FETs, etc.) are under research. But transition is hard and slow. [Wikipedia+2InSemi Tech+2](#)

#### 4. Architecture / software shifts

- Because scaling transistor density becomes harder, designers are increasingly relying on other ways to improve “effective performance”: smarter architecture (e.g., more parallelism, specialized accelerators, heterogeneous computing), software optimizations, hardware-software co-design. [Splunk+2arXiv+2](#)

### Signs that Moore’s Law (or something like it) might yet continue

Even with the headwinds, there are reasons to believe that progress can continue, albeit with modifications.

- **Advance of lithography, new nodes**

The industry is pushing process nodes beyond 3nm, working toward 2nm and even concepts like “1nm node range.” [InSemi Tech+4Wikipedia+4Wikipedia+4](#)

- **Innovative transistor architectures**

Gate-All-Around, nanosheets, 3D stacking, vertical transistors, multi-gate designs etc. are helping to offset some of scaling challenges. [PatentPC+2InSemi Tech+2](#)

- **Alternative technologies / post-Moore paradigms**

Research into spintronics, quantum computing, neuromorphic computing, photonics, new materials, etc., may extend or move beyond the straight-line transistor doubling paradigm. While these are further from mass production, they are parts of many roadmaps.

[Wikipedia+2arXiv+2](#)

- **Economic & incentive structure**

Moore’s Law has become a guiding benchmark; companies and governments invest heavily in R&D, fabs, materials, tooling to push the boundaries. There is strong incentive (market demand, AI, HPC, mobile) to continue squeezing out performance and efficiency.

### Outlook: What seems likely for 2025–2035

Putting it all together, here is a rough forecast of what experts expect, with caveats.

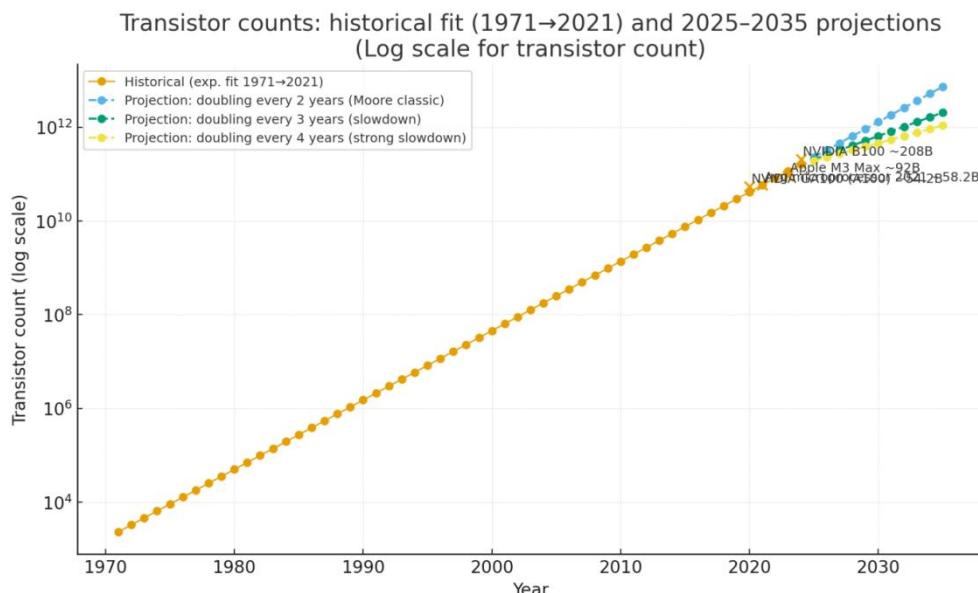
Expectation	Likelihood / Confidence	Key Implications
Transistor density will continue to increase, but <b>not at the same rate</b> (i.e. doubling every two years will likely slow)	High	Slower cadence of new process nodes; node transitions cost more; performance improvements become more incremental.
Cost per transistor improvements will flatten (or even increase in some cases) for the leading edge	High	Chip makers and OEMs will see rising costs; margins or pricing may need to adjust; more selective where leading-edge is used vs mid/low end.
More emphasis on architecture, specialization, asymmetric computing, accelerators, ML-specific chips	Very High	Benefit from co-design, domain-specific hardware, data flow optimizations; hardware will be more “bespoke.”
More heterogeneous integration, 3D stacking, chiplets, packaging innovations	High	To bypass some interconnect and density limitations, systems will use more vertical/integrated approaches and modular chip combinations.
Research into alternative materials / paradigms will get more funding and perhaps see some breakthroughs	Moderate	Some may reach manufacturing scale for niche uses; general replacement of silicon logic at scale remains uncertain during this period.

Expectation	Likelihood / Confidence	Key Implications
For many applications (consumer, mobile, edge), “good enough” improvements (efficiency, power, cost) will remain more important than pure density or raw GHz	Very High	Design trade-offs will favor energy, thermal limits, integration, cost; not just peak speed or transistor count.

## Conclusion

In conclusion: **Moore’s Law in its original formulation (doubling transistor count every ~2 years with a matching drop in cost) is increasingly under pressure**, and many of the gains are slowing. But the broader trend of exponential improvement in computing capabilities is unlikely to disappear soon—it’s just that the mechanisms will shift more toward innovation in architecture, materials, packaging, and system-level design, rather than pure transistor scaling.

Quantitative forecasts (e.g. projections for transistor density, performance, power consumption) for 2025-2035 to see how sharp the slowdown might be.



*The chart that shows a historical exponential fit for transistor counts (1971→2021 anchor) and three projection scenarios for 2025–2035: (compiled by chatGPT)*

- Classic Moore: transistor count doubles every **2 years** (the original rule of thumb).
- Slowdown: doubling every **3 years**.
- Strong slowdown: doubling every **4 years**.

I also overlaid a few recent datapoints for context (A100, Apple M3 Max, NVIDIA B100) so you can see how leading-edge chips compare to the average-per-microprocessor curve.

## Notes, assumptions and sources

- The historical fit is an exponential interpolation anchored to Our World in Data’s summary values: **~2,308 transistors (1971)** and **~58.2 billion (2021)** — OWID reports an average doubling time  $\approx 2.03$  years over 1971–2021. Our World in Data [+1](#)

- Recent representative chip datapoints are used for reference (not as part of the fitted history): NVIDIA GA100 / A100 ~**54.2B** transistors (NVIDIA whitepaper), Apple M3 Max ~**92B** (Apple announcement), NVIDIA B100 ~**208B** (industry reporting). [Apple +2](https://images.nvidia.com/+2)
- Additional context about transistor **density** trends and technical limits (why pure scaling is getting harder and why people talk about “Moore is slowing”) is discussed in IEEE Spectrum and other industry sources. IEEE Spectrum [+1](#)

### Interpretation — what the chart tells us (brief)

- Historical exponential growth (1971→2021) maps closely to “Moore-like” behavior overall — that’s why the law has been useful as a heuristic. Our World in Data
- If the industry were to continue the classic doubling every 2 years from the 2024 baseline, transistor counts would rise steeply by 2035 (blue dashed line). If instead scaling slows to doubling every 3–4 years, counts in 2035 would be substantially lower (green/yellow lines). Those slower scenarios are plausible given rising fab costs and physical/material limits; conversely, packaging (chiplets, 3D stacking), heterogeneous accelerators, and wafer-scale approaches can push “effective compute” beyond raw transistor counts. IEEE Spectrum [+1](#)

October 2025, Joachim J. Kehr, Editor Journal of spaceOperations & Communicator  
<https://opsjournal.org>